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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/579,911	04/09/2007	Satoru Hanzawa	XA-10573	6903

181 7590 01/06/2009

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EXAMINER	
HIDALGO, FERNANDO N	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
01/06/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/579,911	HANZAWA ET AL.	
	Examiner	Art Unit	
	FERNANDO N. HIDALGO	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Drawings

1. The drawings were received on 10/6/08. These drawings are acceptable.

Claim Objections

2. Previous claim(s) objections are moot in view of the claim amendments as filed on 10/6/08.

3. Applicant's arguments substantially with respect to independent claim(s) 11, 16 and 18 have been considered but are moot in view of the new ground(s) of rejection. Furthermore, the remarks concede that amendments to claim 11 are amended "for clarity." That is there is no substantive change in the claim language as amended. As such the previous ground of rejection for independent claim 11 and dependent claims 12-15 of said independent claim hold. Claim 16, as amended, introduces language describing obvious, as known in the art and to one of ordinary skill in said art, physical processing and layout attributes of semiconductor transistors and connectivity of same with semiconductor traces such as polysilicon and/or metal traces well known in the abundantly large body of semiconductor knowledge. For further reference, refer to the claim rejections below.

Allowable Subject Matter

4. **Claim 18** is allowed.

5. The following is an examiner's statement of reasons for allowance: the pertinent prior art of record does not teach or suggest, in combination with the rest of the claim limitations, a semiconductor integrated circuit device comprising: " wherein a voltage supplied to the plurality of bit lines pairs varies between a first voltage and a second voltage lower than the first voltage, wherein a voltage supplied to the plurality of search line pairs varies between a third voltage and a fourth voltage lower than the third voltage, wherein the first voltage is larger than the third voltage."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. **Claim 19** depends on independent claim 19 and is therefore allowed for at least the same reasons.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claim 20** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. **Claim 20** recites the limitation "wherein the second voltage and the forth voltage are the same" in lines 3-4 of said claim. There is insufficient antecedent basis for this limitation in the claim.

10. **Claim(s) 1-10** have been cancelled by the applicant.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claim(s) 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6343029 B1 to Kengeri et al. ("Kengeri") in view of U.S. Publication 66MHz 2.3M Ternary Dynamic Content Addressable Memory to Lines et al. ("Lines").

As to **claim 11**, Kengeri discloses a semiconductor integrated circuit device wherein each of the match line pairs has a precharge circuit (FIG. 1 shows each of the match line pairs ML and SL have pre-charge circuits 181 and 182, respectively); the precharge circuit drives the first match line of the match line pair to the first voltage and the second match line thereof to the second voltage lower than the first voltage, respectively (FIG. 1 shows that first pre-charge circuit 181 drives match line ML to first voltage Vc and second pre-charge circuit drives match line SL to GND, which is lower than the first voltage, respectively); each of the memory cells has a storage circuit and a comparator (FIG. 1 shows storage circuit 191 and comparator 110; also see Column 2, lines 52-65); each of the comparators has the first and the second MOS transistors (FIG. 4 shows comparator 110 having a first and a second MOS transistors 113,

114); gate electrodes of the first and second MOS transistors are connected to the search lines, respectively (FIG. 4 shows that gates of 113 and 114 are connected to search lines DLA and DLB, respectively); and the second match line is put in a floating state when comparison operation is performed in the comparator (FIG. 1, Column 1, lines 47-67 disclose that the second latch line SL is put in a floating state when in comparison operations; that is disclosed is that SL is pre-charged to ground, prior to a comparison operation, and in response to a data mismatch detected by the comparator, the first match line voltage is put on charge-sharing with the SL match voltage, as pre-charged, and consequently the first match voltage is prevented to discharge to ground. This discharge to ground, inherently, can only happen if the second match line had been connected to ground; charge sharing can only take place between two signal voltages able to drive one-another).

Kengeri does not expressly disclose a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs; one of a source electrode and a drain electrodes of the first and second MOS transistors is connected to the associated first match line.

Lines teaches a plurality of match line pairs (FIG. 2 shows a memory cell with a pair of match lines, and FIG. 1 shows an exemplary memory array floor plan of the memory cells in FIG. 2; thus a plurality of match lines), a plurality of

search line pairs intersecting the plurality of match line pairs (FIG. 2 shows a memory cell with a pair of search lines, and FIG. 1 shows an exemplary memory array floor plan of the memory cells in FIG. 2; thus a plurality of search lines), and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs (FIG. 2 shows a memory cell arranged with a pair of match lines and search lines, and FIG. 1 shows an exemplary memory array floor plan of the memory cells in FIG. 2; thus a plurality of cells arranged as in FIG. 2; alternatively FIG. 3 shows a plurality of memory cells as in FIG. 2); either of source or drain electrodes of the first and second MOS transistors are connected to the first match line (FIG. 2 shows a memory cell, wherein the source/drain of the first and second MOS transistors M3, M5 are connected to the first match line ML).

Kengeri and Lines are analogous art because they are from the same field of endeavor regarding semiconductor memory circuit design, more specifically Content addressable memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to provide a plurality of match line pairs, a plurality of search line pairs intersecting the plurality of match line pairs, and a plurality of memory cells arranged at intersecting points of the plurality of match line pairs with the plurality of search line pairs; either of source or drain electrodes of the first and second MOS transistors are connected to the first match line as taught by Lines in the above claim limitation rejection. The suggestion/motivation would

have been obvious to one of ordinary skill in the art in providing a memory array comprising a plurality of memory cells; while Kengeri discloses his invention with a cell as the focal point, it is obvious to one of ordinary skill that practical realization of the invention encompasses a memory array device. Furthermore, Kengeri' comparator and Lines' comparator cell differ only in the match line that is connected to the first and second MOS transistors. One advantage Lines has with his comparator is that first and second MOS transistors de-couple the devices driven by the storage cells from a dynamically operational first match line, as influenced by search line dynamic activity. This inherently reduces the coupling of the storage cells with the dynamically changing first match line and thus prevents undue charge influence on the storage elements from dynamic changes on the first match line.

Therefore, it would have been obvious to combine Kengeri with Lines to make the above modification.

As to **claim 12**, Kengeri discloses that a source - drain path in the first MOS transistor is included in the first current path between the first and the second match lines (FIG. 1 shows that source/drain of the first transistor 113 is included in the first current path between first match line ML and second match line SL); a source - drain path in the second MOS transistor is included in the second current path between the first and the second match lines (FIG. 1 shows that source/drain of the second transistor 114 is included in the second current path between first match line ML and second match line SL); the comparator

generates a signal voltage corresponding to a result of comparing data stored at the storage circuit and data inputted via the search lines at the match line (FIG. 1 shows that in response to data inputted on the search lines DLA and DLB and data stored on storage circuits 191 and 192, comparator 110 generates signal voltage on first match line ML).

13. **Claim(s) 13-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6343029 B1 to Kengeri et al. ("Kengeri") in view of U.S. Publication 66MHz 2.3M Ternary Dynamic Content Addressable Memory to Lines et al. ("Lines"), further in view of U.S. Patent No. 6483733 B2 to Lines et al. ("Lines-2").

As to **claim 13**, Kengeri, as modified, discloses substantially the claimed invention except that the first and the second coupling capacitances being parasitic between the search line and the first match line are larger than the third and the fourth coupling capacitances being parasitic between the search line and the second match line.

Lines-2 teaches that the first and the second coupling capacitances being parasitic between the search line and the first match line are larger than the third and the fourth coupling capacitances being parasitic between the search line and the second match line (FIG. 2 shows an exemplary memory cell and comparator having a first match line ML, a second match line DL and first and second search lines SL1 and SL2; FIG 6B shows a circuit mask layout of FIG. 2, wherein it is shown that the parasitic capacitance (not shown, but inherently available and thus operable to be analyzed) between the first match line ML and the search

line SL2 is larger than the parasitic capacitance between the second match line DL and the search line SL2as follows: the first match line ML is much closer in proximity to search line SL2 resulting in a larger parasitic capacitance, the proximity of the second match line to the search line is plainly observable to be not as close, thus resulting in a smaller coupling parasitic capacitance; as well known in the art, capacitance is inversely proportional to the distance between two conductive elements).

For suggestion/motivation to combine, see rejection to claim 11.

As to **claim 14**, Kengeri, as modified, discloses substantially the claimed invention except a match detector is arranged in each of the second match lines; and the match detector determines the data-comparison results by discriminating voltages of the second match line.

Lines teaches a match detector is arranged in each of the second match lines; and the match detector determines the data-comparison result by discriminating voltages of the second match line (FIG. 4 shows a match detector sense amplifier circuitry, wherein the match line ML voltage, as it changes depending on a match or mismatch, determines the result from the comparator of FIG. 2 by noticing differences, discriminating voltages on the second match line as follows: as seen on FIG. 2, the comparison result of the comparator as available on the first match line ML, is highly dependent on the voltage value expectancy of the second match line ML_VSS; depending on a data match or

mismatch, the first mach line voltage value will reach a value by discriminating the value of the second match line via devices M3-M6).

For suggestion/motivation to combine, see rejection to claim 11; further, it would have been obvious to provide a means to detect to comparison value as generated by the cell/comparator for amplification and further data processing as well done and practiced in applications using memory devices in general.

As to **claim 15**, Kengeri, as modified, discloses substantially the claimed invention except that the storage circuit has two transistors and two capacitors.

Lines teaches that the storage circuit has two transistors and two capacitors (FIG. 2 shows two transistors M1 and M2 and two capacitors C1 and C2).

Kengeri and Lines are analogous art because they are from the same field of endeavor regarding semiconductor memory circuit design, more specifically Content addressable memory.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to provide that the storage circuit has two transistors and two capacitors as taught by Lines in the above claim limitation rejection. The suggestion/motivation would have been to use DRAM technology for the basic cell to provide large density memory in a comparably reduced semiconductor area (See Abstract).

Therefore, it would have been obvious to combine Kengeri with Lines to make the above modification.

14. **Claim(s) 16-17 are** rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6343029 B1 to Kengeri et al. ("Kengeri") in view of U.S. Publication 66MHz 2.3M Ternary Dynamic Content Addressable Memory to Lines et al. ("Lines"), U.S. Patent No. 6483733 B2 to Lines et al. ("Lines-2"), and further in view of Analog Integrated Circuit Design to Johns et al. ("Johns").

As to **claim 16**, see rejection to claim 11, furthermore, Kengeri discloses that the comparator comprises the first and the second MOS transistors connected serially so as to form the first current path between the first and the second match lines (FIG. 1 shows first and second MOS transistors 111 and 113 between the first match line ML and second match line SL forming a current path), and the third and the fourth MOS transistors connected serially so as to form the second current path (FIG. 1 shows third and fourth MOS transistors 112 and 114 between the first match line ML and second match line SL forming a second current path).

Lines teaches gate electrodes of the first and third MOS transistors are connected to the search lines, respectively (FIG. 2 shows that first and third MOS transistors M3 and M5 have gates connected to search lines SL1bb and SL2b, respectively); either of electrodes of source or drain electrodes of the first and the third MOS transistors are connected to the first match lines through contacts formed through self- aligned process (FIG. 2 shows drain/source of first and third MOS transistors connected to first match line ML by making use of DRAM technology which enables a smaller memory cell foot-print, see Abstract); gate

electrodes of the second and fourth MOS transistors are connected to the storage circuits, respectively (FIG. 2 shows gate electrodes of the second and fourth MOS transistors M4 and M6 connected to storage elements C1 and C2, respectively); and either of electrodes of source or drain electrodes of the second and fourth MOS transistors are connected to the second match lines through contacts formed through self- aligning process (FIG. 2 shows that drain/source of second and fourth MOS transistors are connected to second match line by making use of DRAM technology which enables a smaller memory cell foot-print, see Abstract)

Alternatively Lines-2 teaches a memory cell (FIG. 2) wherein first and third MOS transistors connect to the first match line ML and second and fourth MOS transistors connect to second match line DL also using DRAM technology.

Furthermore, Johns teaches for each of the first MOS transistor and the third MOS transistor, one of a source electrode and a drain electrode is connected to the associated first match line through a first contact having a lower surface contacting said one source and drain electrode and an upper surface contacted with the first match line; wherein, for each of the second MOS transistor and the fourth MOS transistor, one of a source electrode and a drain electrode is connected to the associated second match line through a second contact having a lower surface contacting said one source and drain electrode and an upper surface contacting the associated second match line, wherein the lower surface of the first contact is smaller than the upper surface of the first

contact, and wherein the lower surface of the second contact is smaller than the upper surface of the second contact (Page 94, FIG. 2-11 illustrates a typical cross sectional view of processing and layout of transistors connecting one of a source and a drain to an associated upper surface metal trace or runner: for example, N-type MOS transistor or P-type MOS transistor, right and left, respectively on FIG. 2-11, connect a source or drain lower surface to trough a "contact," as well known in the art and to an upper surface contacting a metal trace through a "via," as well known in the art; also setting aside the redundancy of the subject matter being extremely well known in the art, the upper surface (via) has a larger surface area than the lower surface contact, as illustrated, and in view of the electrically advantageously property of having a small source/drain surface are to enhance said electrical properties of functionality of said transistors; furthermore, said upper surface contact (via) having a larger surface area to enhance connectivity by reducing resistivity).

For at least the reasons cited above, it would have been obvious to one of ordinary skill in the art to combine Kengeri, Lines, lines-2 and Johns to make the above modification.

As to **claim 17**, Kengeri as modified teaches substantially the claimed invention except that first and second parasitic coupling capacitances between respective search lines of a search line pair and the associated first match lines are generated by an interlayer insulator formed between the first contact and the respective gate electrodes of the associated first and third MOS transistors,

wherein third and fourth parasitic coupling capacitances between respective search lines of the search line pair and the associated second match lines are generated by an interlayer insulator formed between a first metal layer used to form the plurality of search line pairs and a second metal layer used to form the plurality of second match lines, and wherein the first and the second parasitic coupling capacitances are larger than the third and the fourth parasitic coupling capacitances, respectively.

Johns teaches that first and second parasitic coupling capacitances between respective search lines of a search line pair and the associated first match lines are generated by an interlayer insulator formed between the first contact and the respective gate electrodes of the associated first and third MOS transistors, wherein third and fourth parasitic coupling capacitances between respective search lines of the search line pair and the associated second match lines are generated by an interlayer insulator formed between a first metal layer used to form the plurality of search line pairs and a second metal layer used to form the plurality of second match lines, and wherein the first and the second parasitic coupling capacitances are larger than the third and the fourth parasitic coupling capacitances, respectively (Page 94, FIG. 2-11 illustrates a typical cross sectional view of processing and layout of transistors and metal traces or runners connecting the source/drain of said transistors (shown are an N-type MOS and a P-type MOS transistors) to said metal traces (at least metal 1 and metal 2 being as well known in the art above the metal 1, which in turn is above the

source/drain of said transistors); as illustrated at a intersection between a source/drain terminal of a transistor and a metal trace contacting a gate of a transistor there is an interlayer insulator SiO_2 having a first height and thus since capacitance value is inversely proportional to the height of the insulator, for example SiO_2, separating the two conductive traces of the capacitor, and given that this first height is smaller than a second height of wherein a metal 2 trace is involved, as illustrated in FIG. 2-11, then the capacitance value associated with the insulation having a small height is larger than the capacitance value associated with the insulator having a larger height; Fig 2.11 exemplarily illustrates said first and second insulator heights between a source/drain and metal 1 and between metal 1 and metal 2).

For suggestion/motivation to combine, see rejection to claim 16.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N. HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached on Monday-Friday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando N. Hidalgo/
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